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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
BECK, ALEXANDER S	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,545	OSAME ET AL.	
	Examiner	Art Unit	
	ALEXANDER S. BECK	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Apr. 25, 2008, has been entered. Claims 1-33 are currently pending and an Office action on the merits follows.

Information Disclosure Statement

2. The information disclosure statement filed Mar. 24, 2008, has been acknowledged and considered by the examiner. An initialed copy of the PTO-1449 is included in this correspondence.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were

made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 4, 6-10, 12-14, 18, 22-24, 26, 27, 29-31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2001/0002703 by Koyama ("Koyama").

As to claim 1, Koyama discloses a light emitting device comprising: a pixel (Koyama, 104) (Koyama, ¶ [0115]) comprising: a light-emitting element (Koyama, 111) (Koyama, ¶ [0116]), a first transistor (Koyama, 112) for determining a value of a current flowing to the light-emitting element (Koyama, ¶ [0117]), and a second transistor (Koyama, 109) for determining a light emission or non light emission of the light-emitting element depending on a video signal input to a signal line (Koyama, 107) (Koyama, ¶ [0117]), wherein the light-emitting element, the first transistor, and the second transistor are connected in series between a first power line (Koyama, 110) and a counter electrode of the light-emitting element, wherein a gate electrode of the first transistor is connected to a second power line (Koyama, 113) (Koyama, Fig. 3), wherein the signal line, the first power line, and the second power line are provided in parallel with each other (Koyama, ¶ [0115]; see also Fig. 3).

As noted above, Koyama discloses wherein the signal line (Koyama, 107), the first power line (Koyama, 110), and the second power line (Koyama, 113) are provided in parallel with each other (Koyama, ¶ [0115]; see also Fig. 3). Although Koyama does not disclose expressly the order of these three lines per pixel, there are three possibilities: 1) the first power line is provided between the signal line and the second power line; 2) the

second power line is provided between the signal line and the first power line; and 3) the signal line is provided between the first power line and the second power line. Thus, Koyama does not disclose expressly wherein the first power line is provided between the signal line and the second power line, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify Koyama such That the first power line is provided between the signal line and the second power line because applicant has not disclosed that such a specific configuration provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with having the signal line, first power line, and second power line in parallel with one another in a different order (e.g., any one of those suggested by Koyama) because both would perform equally well in driving the various transistors in a pixel of a display device.

As to claim 2, all of the limitations have already been discussed in the rejection of claim 1 above with the exception of: a third transistor for controlling an input of the video signal. Koyama discloses the pixel (Koyama, 104) comprising a third transistor (Koyama, 105) for controlling an input of the video signal (Koyama, ¶ [0116]; see also Fig. 3).

As to claim 8, all of the limitations have already been discussed in the rejection of claim 1 above. Furthermore, Koyama discloses an element substrate comprising the pixel of claim 1 (Koyama, ¶ [0106]) and the claimed "pixel electrode" is rejected in the same manner as the "light emitting element" in claim 1.

As to claims 4 and 14, Koyama discloses wherein the first transistor and the second transistor are identical in conductivity (e.g., can be both p-channel or n-channel transistors) (Koyama, ¶¶ [0113-118, 148-152]).

As to claims 6 and 7, Koyama discloses the first transistor and second transistor having a channel length and a channel width (e.g., implicitly suggested in thin film transistors). However, Koyama does not disclose expressly wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal to or shorter than a channel width, wherein a ratio of the channel length to the channel width of the first transistor is 5 more, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the first transistor and second transistor had channel widths/lengths as claimed because applicant has not disclosed that such a specific transistor channel length/width provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor channel width/length because both would perform equally well in functioning as switches in a pixel of a display device.

As to claim 9, Koyama discloses wherein each of the first transistor and the second transistor has P-type conductivity (Koyama, ¶¶ [0150-0152]) wherein each transistor has a threshold value (e.g., implicitly suggested in a transistor). However, Koyama does not disclose wherein a threshold value of the first transistor is higher than that of the second transistor, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the threshold value of the first transistor is higher than that of the second transistor as claimed because applicant has not disclosed that such a specific threshold value relationship provides an advantage, is used for a particular purpose, or solves a

stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor threshold value relationship for a pixel in a display device because both would perform equally well in functioning as switches in a pixel of a display device.

As to claim 10, Koyama discloses wherein each of the first transistor and the second transistor has an N-type conductivity (Koyama, ¶¶ [0150-0152]) wherein each transistor has a threshold value (e.g., implicitly suggested in a transistor). However, Koyama does not disclose expressly wherein a threshold value of the first transistor is lower than that of the second transistor, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the threshold value of the first transistor is lower than that of the second transistor as claimed because applicant has not disclosed that such a specific threshold value relationship provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor threshold value relationship for a pixel in a display device because both would perform equally well in functioning as switches in a pixel of a display device.

As to claims 12 and 13, all of the claim limitations have already been discussed in the rejection of claims 6 and 7 above.

As to claims 18 and 24, all of the claim limitations have already been discussed in the rejection of claims 6 and 7 above.

As to claims 22 and 23, all of the claim limitations have already been discussed in the rejection of claims 6 and 7 above.

As to claims 26, 27 and 29, Koyama discloses wherein the light-emitting device (or element substrate) is incorporated into at least one selected from the group consisting of a cellular phone, a mobile computer, a game machine, an electronic book, a video camera, a digital camera, a goggle display, a display device, and a navigation system (Koyama, ¶ [0002]).

As to claims 30, 31 and 33, Koyama discloses wherein a potential of the gate electrode of the first transistor (Koyama, 112) is fixed (Koyama, ¶ [0139]).

6. Claims 5, 11, 16, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama as applied to claims 1, 2, 4, 6-10, 12-14, 18, 22-24, 26, 27, 29-31 and 33 above, and further in view of U.S. Patent No. 6,207,969 to Yamazaki ("Yamazaki").

As to claims 5, 11, 16, 20 and 21, Koyama does not disclose expressly wherein the first transistor comprises a depletion type, as claimed. Yamazaki discloses a light-emitting device comprising a depletion type transistor for driving a light-emitting element (Koyama, Figs. 1-2B, 14; see also col. 1, ll. 13-15 and 46-53). At the time the invention was made, it would have been obvious to one having ordinary skill in the art to further modify the teachings of Koyama such that the first transistor is a depletion type, as taught by Yamazaki. The suggestion/motivation for doing so would have been so that the transistor could be formed on a single crystal silicon film by an intrinsic semiconductor in a silicon on insulator (Yamazaki, col. 1, ll. 45-53), as one of ordinary skill in the art would appreciate.

7. Claims 3, 15, 19, 25, 28 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama in view of U.S. Patent Publication No. 2002/0113760 by Kimura ("Kimura").

As to claim 3, all of the limitations have already been discussed in the rejection of claims 1 and 2 above with the exception of: a fourth transistor for forcing the light-emitting element into a non-emission state irrelevant from the video signal, as claimed. Koyama does not disclose expressly this limitation.

Kimura discloses a pixel (Kimura, 732) for a light-emitting device comprising a fourth transistor (Kimura, 740) for forcing a light-emitting element (Kimura, 738) into a non-emission state irrelevant from the video signal (Kimura, Fig. 17B; see also ¶ [0150-0160]). At the time the invention was made, it would have been obvious to one having ordinary skill in the art to further modify the teachings of Kimura such that a pixel of the light-emitting device comprised a fourth transistor, as taught by Kimura. The suggestion/motivation for doing so would have been to display an image without decreasing a frame frequency if the number of bits of a digital signal is increased (Kimura, ¶ [02160]), as one of ordinary skill in the art would appreciate.

As to claim 15, all of the limitations have already been discussed in the rejection of claims 4 and 14 above.

As to claims 19 and 25, all of the limitations have already been discussed in the rejection of claims 6 and 7 above.

As to claim 28, all of the limitations have already been discussed in the rejection of claims 26, 27 and 29 above.

As to claim 32, all of the limitations have already been discussed in the rejection of claims 30, 31 and 33 above.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama and Kimura as applied to claims 3, 15, 28 and 32 above, and further in view of Yamazaki.

As to claim 17, Koyama does not disclose expressly wherein the first transistor comprises a depletion type, as claimed. Yamazaki discloses a light-emitting device comprising a depletion type transistor for driving a light-emitting element (Koyama, Figs. 1-2B, 14; see also col. 1, ll. 13-15 and 46-53). At the time the invention was made, it would have been obvious to one having ordinary skill in the art to further modify the teachings of Koyama such that the first transistor is a depletion type, as taught by Yamazaki. The suggestion/motivation for doing so would have been so that the transistor could be formed on a single crystal silicon film by an intrinsic semiconductor in a silicon on insulator (Yamazaki, col. 1, ll. 45-53), as one of ordinary skill in the art would appreciate.

Response to Arguments

Applicant's arguments filed Apr. 25, 2008, with respect to the rejection of independent claims 1-3 and 8 have been fully considered but they are not persuasive. Examiner respectfully submits that the arguments have been addressed in the rejections above. For example, applicant argues that Koyama does not teach or suggest a signal line, a first power line, and a second power line in parallel with each other, where the first power line is provided between the signal line and the second power line.

However, examiner respectfully submits that Koyama discloses wherein the signal line (Koyama, 107), the first power line (Koyama, 110), and the second power line (Koyama, 113) are provided in parallel with each other (Koyama, ¶ [0115]; see also Fig. 3). Although Koyama does not disclose expressly the order of these three lines per pixel, there are three possibilities: 1) the first power line is provided between the signal line and the second power line; 2) the second power line is provided between the signal line and the first power line; and 3) the signal line is provided between the first power line and the second power line. Thus, Koyama does not disclose expressly wherein the first power line is provided between the signal line and the second power line, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify Koyama such That the first power line is provided between the signal line and the second power line because applicant has not disclosed that such a specific configuration provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with having the signal line, first power line, and second power line in parallel with one another in a different order (e.g., any one of those suggested by Koyama) because both would perform equally well in driving the various transistors in a pixel of a display device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER S. BECK whose telephone number is (571)272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander S. Beck/
Examiner, Art Unit 2629